Remarks

The Office Action dated April 9, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 30 and 47 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1 - 48 are pending in the present application and are respectfully submitted for consideration.

Claims 18-21, 24-26, 28, 30 and 31 were rejected under 35 U.S.C. § 102(b) as being anticipated by JP-05053857 A (hereinafter "JP '857"). Applicant respectfully traverses this rejection and submits that each of claims 18-21, 24-26, 28, 30 and 31 recites subject matter that is neither disclosed nor suggested in this cited prior art.

As a preliminary matter, Applicant submits an English translation of JP '857 to better support the arguments set forth below. Specifically, Applicant submits that the original cited reference of JP '857 contains errors in paragraphs [0017] and [0019]. In other words, the subject matter discussed in paragraphs [0017] and [0019] of JP '857 is incorrect and the translation of JP '857 submitted herewith is a translation with the incorrect subject matter. Rather, it is submitted that paragraphs [0017] and [0019] of JP '857 should be read as follows in consideration of an inversion function of an input buffer 1.

[0017] If either of the lines 103 and 104 that connect the LSI-A10 and the LSI-B20 is disconnected, the signal supplied to the input buffer 1 is always set to ~~"1"~~ "0". As

the result, the test data supplied from the input buffer 1 and stored in the test data register 2 via the line 105 is always set to "1".

[0019] Alternatively, if the signal supplied to the input buffer 1 is always set to ~~"0"~~ "1" due to the disconnection of either of the lines 103 and 104, the data supplied from the input buffer 1 to the test data register 2 via the line 5 is always set to "0".

Therefore, the corrections noted above with respect to the cited reference should be taken into consideration with the arguments set forth below.

Claim 18 recites an electronic device having first and second semiconductor devices connected to each other with a plurality of bus lines. The first semiconductor device includes a first output circuit connected to one of the bus lines for supplying the bus line with a first logical output signal, an inversion output circuit connected to the bus line for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal, and a comparison circuit connected to the bus line. The second semiconductor device includes an input circuit connected to the bus line for acquiring a first bus line signal, and a second output circuit connected to the input circuit for supplying a corresponding bus line with the first bus line signal. The comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

Claim 24 recites a first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto

with bus lines. The first semiconductor device includes an output circuit connected to each bus line that supplies each bus line with a first logical output signal. The second semiconductor device receives a first bus line signal and supplies a bus line with a second logical output signal being an inverted signal of the first bus line signal. The first semiconductor device also includes a comparison circuit connected to each bus line that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

Claim 25 recites a first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with bus lines. The first semiconductor device includes an output circuit connected to each bus line that supplies each bus line with a first logical output signal. The second semiconductor device receives a first bus line signal. The first semiconductor device also includes an inversion output circuit connected to each bus line that supplies each bus line with a second logical output signal being an inverted signal of the first logical output signal after the output circuit supplying the first logical output signal, and a comparison circuit connected to each bus line that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

Claim 30 recites the semiconductor device having input terminals, output terminals, an internal circuit, first bus lines that connect the input terminals and the

internal circuit, respectively, and second bus lines that connect the output terminals and the internal circuit, respectively. In addition, the semiconductor device includes test circuits connected between either the first bus lines and the output terminals, or the second bus lines and the input terminals. The test circuits are activated in a test mode and are deactivated in a normal operation mode in order to share the first bus lines or the second bus lines in both of the test mode and the normal operation mode.

Accordingly, at least one of the essential features of the present invention is a an inversion output circuit connected to the bus line for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal. As such, the present invention results in the advantage of decreasing the circuit area for testing which increases the efficiency of the present invention.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims, and therefore fails to provide the advantages which are provided by the present invention.

JP '857 discloses a circuit for testing connection between LSI. The circuit is equipped with a test data register 2 to invert a signal between LSIs from an LSI-B 20 and to store the signal in an LSI-A10, a comparison register 4 to store the inverted output of this test data register 2, a comparator 5 to compare the contents of the test data 2 with the contents of the comparison register 4, and loops 1, 3, 6 and 7 to transmit the LSI-A10 and the LSI-B20 and to return the data to the original test data register 2 after inverting them while being equipped with the test data register 2.

Applicant respectfully submits that each and every element recited within claims 18, 24, 25 and 30 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the test method and test circuit for an electronic device as recited in the present application is clearly distinct from that which is illustrated in JP '857.

Applicant submits that claimed invention recited in claims 18, 24 and 25 of the present application is neither comparable nor analogous to JP '857 for at least the following two reasons:

(1) JP '857 performs a connection check of two lines between 2 LSIs and does not perform a connection check of bus lines; and

(2) JP '857 fails to show transferring of inverted data from a first semiconductor device to a second semiconductor device or from the second semiconductor device to the first semiconductor device.

Given the above regarding JP '857, the following drawbacks may occur when the bus lines are applied.

When a test register 2 of an LSI-A provides data "0" to an LSI-B, data "1" inverted by an inverter 3 is set in a comparison register 4. Then, the LSI-B receives the data "0" from the LSI-A. At this time, when one or more of bus lines are disconnected, the data "0" is maintained (not changed to "1") due to line capacitance of the bus lines. Accordingly, the data "0" is returned to the LSI-A and data "1" inverted by the inverter 3 is set in the test register 2. A comparator 5 compares the inverted data "1" set in the comparison register 4 and the data "1" set in the test register 2 to thereby generate a

comparison result signal "0" indicating that a connection state is normal even if one or more of bus lines are disconnected. Therefore, the test result of JP '857 causes malfunction of a semiconductor device.

In contrast, the claimed invention recited in claims 18, 24 and 25 of the present application provides inverted data from the second semiconductor device to the first semiconductor device, or from the first semiconductor device to the second semiconductor device. For example, when data "0" is transferred from the first semiconductor device to the second semiconductor device in a state where one or more of bus lines are disconnected, the second semiconductor device receives data "0" but not inverted data "1". Accordingly, a comparator of the second semiconductor device compares the transfer data "0" with the received data "0" to determine that one or more of the bus lines are disconnected (in a normal connection state, the transfer data "0" and inverted data "1" are compared). Therefore, Applicant submits that JP '857 fails to disclose or suggest each and every element recited in claims 18, 24 and 25 of the present application, and that claims 18, 24 and 25 are allowable.

As for the rejection with respect to claims 19-21 and 28, it is submitted that claims 19-21 and 28 are dependent claims dependent from independent claim 18. Thus, Applicant respectfully submits that claims 19-21 and 28 are allowable due to their dependency from allowable claim 18.

Applicant further submits that the claimed invention recited in claim 30 of the present application is neither comparable nor analogous to JP '857. Claim 30 is directed to a semiconductor device that includes test circuits connected between either

first bus lines and output terminals, or second bus lines and input terminals. The test circuits of the present invention are activated in a test mode and are deactivated in a normal operation mode. This connection and control of the test circuits allows to share the first bus lines or the second bus lines in both of the test mode and the normal operation mode, thereby reducing a circuit area in the present invention. It is submitted that the cited reference of JP '857 fails to disclose at least such a feature as recited in claim 30. Accordingly, Applicant submits that each and every element recited within claim 30 is neither disclosed nor suggested in JP '857, and claim 30 is allowable.

As for the rejection with respect to claim 31, it is submitted that claim 31 is a dependent claim dependent from independent claim 30. Thus, Applicant respectfully submits that claim 31 is allowable due to its dependency from allowable claim 30.

Claims 1-17, 22, 23, 27, 29 and 32-48 were rejected under 35 U.S.C. § 103(a) as being unpatentable over JP '857. Applicant respectfully traverses this rejection and submits that each of claims 1-17, 22, 23, 27, 29 and 32-48 recites subject matter that is neither disclosed nor suggested in this cited prior art.

Claim 1 recites a method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines. The method includes the step of having the first semiconductor device supplying a selected one of the bus lines with a first logical output signal, and having the second semiconductor device acquiring a first bus line signal from the selected bus line. In addition, the steps include having the second semiconductor device invert the first bus line signal to generate a second logical output signal and transmitting the second logical

output signal to the first semiconductor. The first semiconductor device receives a second bus line signal from the selected bus line, and the first semiconductor device compares the first logical output signal and the second bus line signal to judge a connection between the first semiconductor device and the second semiconductor device.

Claim 6 recites a method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines. The method comprises the steps of having the first semiconductor device apply a selected one of the bus lines with a first logical output signal, and having the second semiconductor device acquire a first bus line signal from the selected bus signal. After outputting the first logical output signal, the first semiconductor device generates a second logical output signal being an inverted signal of the first logical output signal and supplying the selected bus line with a second logical output signal. The second semiconductor device outputs the acquired first bus line signal; the first semiconductor device receives a second bus line signal from the selected bus line. The first semiconductor device further compares the first logical output signal and the received second bus line signal to judge a connection between the first semiconductor device and the second semiconductor device.

Claim 11 recites an electronic device having a first and second semiconductor devices connected to each other with a plurality of bus lines. The first semiconductor device includes a first output circuit connected to one of the bus lines for supplying the bus line with a first logical output signal, and a comparison circuit connected to the bus

line. The second semiconductor device includes an input circuit connected to the bus line for acquiring a first bus line signal, and a second output circuit connected to the input circuit for inverting the first bus line signal to generate a second logical output signal, and supplying a corresponding bus line with the second logical output signal. The comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

Claim 47 recites a semiconductor device having input terminals, output terminals, an internal circuit, and test circuits connected between the input terminals and the output terminals. Furthermore, the semiconductor device includes clamp circuits connected to the input terminals that clamp the respective input terminals to a specific potential that is different from a potential of a test mode signal provided to the respective input terminals in a test mode, and release the clamp at the input terminals in a normal operation mode.

Applicant respectfully submits that each and every element recited within claims 1, 6 and 11 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicant respectfully submits that the test method and test circuit for an electronic device as recited in the present application is clearly distinct from that which is illustrated in JP '857.

In other words, the claimed invention recited in claims 1, 6 and 11 of the present application provides inverted data from the second semiconductor device to the first

semiconductor device, or from the first semiconductor device to the second semiconductor device. For example, when data "0" is transferred from the first semiconductor device to the second semiconductor device in a state where one or more of bus lines are disconnected, the second semiconductor device receives data "0" but not inverted data "1". Accordingly, a comparator of the second semiconductor device compares the transfer data "0" with the received data "0" to determine that one or more of the bus lines are disconnected (in a normal connection state, the transfer data "0" and inverted data "1" are compared). Therefore, Applicant submits that JP '857 fails to disclose or suggest each and every element recited in claims 1, 6 and 11 of the present application for at least the reasons set forth above with respect to claims 18, 24 and 25, that claims 1, 6 and 11 are allowable.

As for the rejection with respect to claims 2-5, 7-10, 12-17, 26 and 27, it is submitted that claims 2-5, 7-10, 12-17, 26 and 27 are dependent claims dependent from independent claims 1, 6 and 11, respectively. Thus, Applicant respectfully submits that claims 2-5, 7-10, 12-17, 26 and 27 are allowable due to their dependency from allowable claims 1, 6 and 11, respectively.

As for the rejection with respect to claims 22, 23 and 29, it is submitted that claims 22, 23 and 29 are dependent claims dependent from independent claim 18. Thus, Applicant respectfully submits that claims 22, 23 and 29 are allowable due to their dependency from allowable claim 18.

As for the rejection with respect to claims 32-46 and 48, it is submitted that claims 32-46 and 48 are dependent claims dependent from independent claim 30.

Thus, Applicant respectfully submits that claims 32-46 and 48 are allowable due to their dependency from allowable claim 30.

As for the rejection of claim 47, it is submitted that each and every element recited in the claimed invention is neither disclosed nor suggested by JP '857. The Examiner stated in the Office Action dated April 9, 2003 that selector 6 and 7 correspond to clamp circuits of the present invention. Applicant respectfully traverses the Examiner's position since the Examiner's understanding is incorrect. Each of the selectors 6 and 7 of JP '857 selects test data in a test mode and selects a logical operation signal. The clamp circuits of the present invention clamp the respective input terminals to a specific potential that is different from a potential of a test mode signal provided to the respective input thermals in a test mode (see Fig. 11-17 of the present specification). According to the present invention, input terminals are clamped to a specific potential (e.g. H level) that is different from a potential of a test mode signal (e.g. L level) provided to the respective input terminals in a test mode. Accordingly, when an L level test mode signal is provided to one or more of the input terminals in a state where lines connected to the input terminals are disconnected and opened, test circuits do not enter a test mode. To enter the test circuits in a test mode, the input terminals are forcibly set to a potential of a test mode signal It is determined that input lines connected to the input terminals are disconnected due to a fact that the test circuits do not enter a test mode. The selector 6 and 7 of the cited reference JP '857 cannot clamp input terminals a specific potential as the third invention. Accordingly,

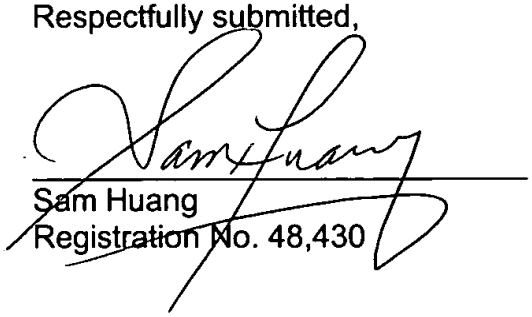
Applicant submits that JP '857 fails to disclose or suggest each and every element recited in the claimed invention.

In view of the above, Applicant respectfully submits that claims 1-48, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully requests that claims 1-48 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-09034.**

Respectfully submitted,



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